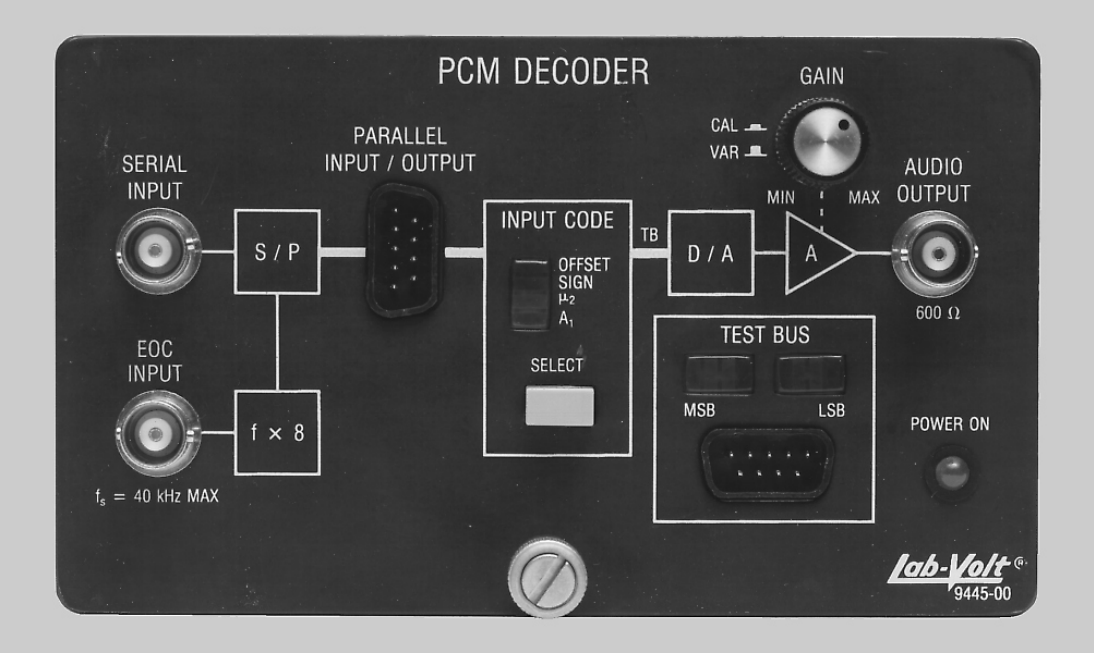
PCM Decoder

Model 9445

Instruction Manual



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INTRODUCTION

The PCM Decoder, Model 9445, is manufactured and tested under strict quality control. If the PCM Decoder requires repair within the warranty period, contact your field representative to obtain instructions for forwarding the module to the nearest authorized Lab-Volt Service Center.

If the PCM Decoder requires repair after the warranty period, it is recommended that it be returned for service.

Note: *The technical information and diagrams in this instruction manual were up to date at the time of publication. It is possible, however, that modifications have since been made in order to improve the product. To have the most up-to-date information, contact your field representative and state both the model and serial numbers.*

Note: *This equipment is for use only in industry and school laboratories where qualified supervision is provided.*

WARRANTY

Lab-Volt warrants all equipment against defects in material and workmanship for a period of one year from the date of installation and/or acceptance by the customer. This warranty covers only the intended use of the equipment and does not cover damage due to alteration, negligent use or normal wear.

We assume no liability for damage, injury or expense claimed to have been incurred through the installation or use of our products.

Questions concerning this warranty and all requests for repairs should be directed to the Lab-Volt field representative in your area.

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SECTION 1

DESCRIPTION

The PCM Decoder, Model 9445, part of the Lab-Volt Digital Communications Training System, has been designed to study pulse code modulation (PCM).

The PCM Decoder is designed to supply an analog voltage proportional to an 8-bit PCM signal. The 8-bit PCM signal can be fed on a parallel input or sequentially on a serial input.

Incoming PCM signal, sequential or parallel can be modified by the PCM Decoder using a ROM for code transposition or expansion. The output of the ROM is fed to the digital-to-analog (D/A) converter and to a test bus.

Before reaching the output of the module, the analog signal of the D/A converter is fed to a variable gain amplifier.

Fault switches located inside the module allow fault insertion.

Eight-bit busses allow troubleshooting or simplify analysis of the system through observation of signals at various stages in the circuit. Access is through a multi-pin connector located on the front panel of the module.

The PCM Decoder, Model 9445, has been designed to be inserted into the Enclosure / Supply Regulator, Model 9420. Regulated power is provided through the backplane connectors of the Enclosure / Supply Regulator mating with the edge connector on the back of the PCM Decoder. The inputs and outputs of the module are protected against all misconnections and short circuits.

A thumb screw securely fastens the module to the Enclosure / Supply Regulator.

SECTION 2

SPECIFICATIONS

Power Requirements	+15 V –50 mA +5 V –360 mA –5 V –2 mA –15 V –50 mA
EOC Input	
Level	TTL
Maximum Frequency	40 kHz
Serial Input	
Level	TTL
Bit Rate	8 x f_{EOC}
Minimum Bit Rate	2400 bps
Maximum Bit Rate	320 kbps
Parallel Input / Output	
Level	TTL
Maximum Transfer Rate	100 k byte/s
Analog Output	
Impedance	600 Ω
Gain (output without load)	
CALibrated	2
VARiable	0-10
D / A Converter	
Input Code	OFFSET
Accuracy (gain in CALibrated mode)	± 1%
Fault Switches	8
Test Bus	1

Note: *The technical information and diagrams in this instruction manual were up to date at the time of publication. It is possible, however, that modifications have since been made in order to improve the product. To have the most up-to-date information, contact us and state both the model and serial numbers.*

Note: *Use only with Power Supply Model 9401.*

Note: *For use only in industry and school laboratories where qualified supervision is provided.*

SECTION 3

OPERATING FEATURES

1 SERIAL INPUT – BNC connector to inject the serial form PCM signal transmitted by the PCM Encoder.

2 PARALLEL INPUT / OUTPUT – Nine-pin connector to provide the output signal from the serial-to-parallel (S/P) converter. This connector also serves to inject the PCM signal if no signal is detected on the EOC INPUT.

3 INPUT CODE – Red LED display used to monitor the selected input code.

4 INPUT CODE SELECT – Push button used to select one of the four input codes accepted by the PCM Decoder.

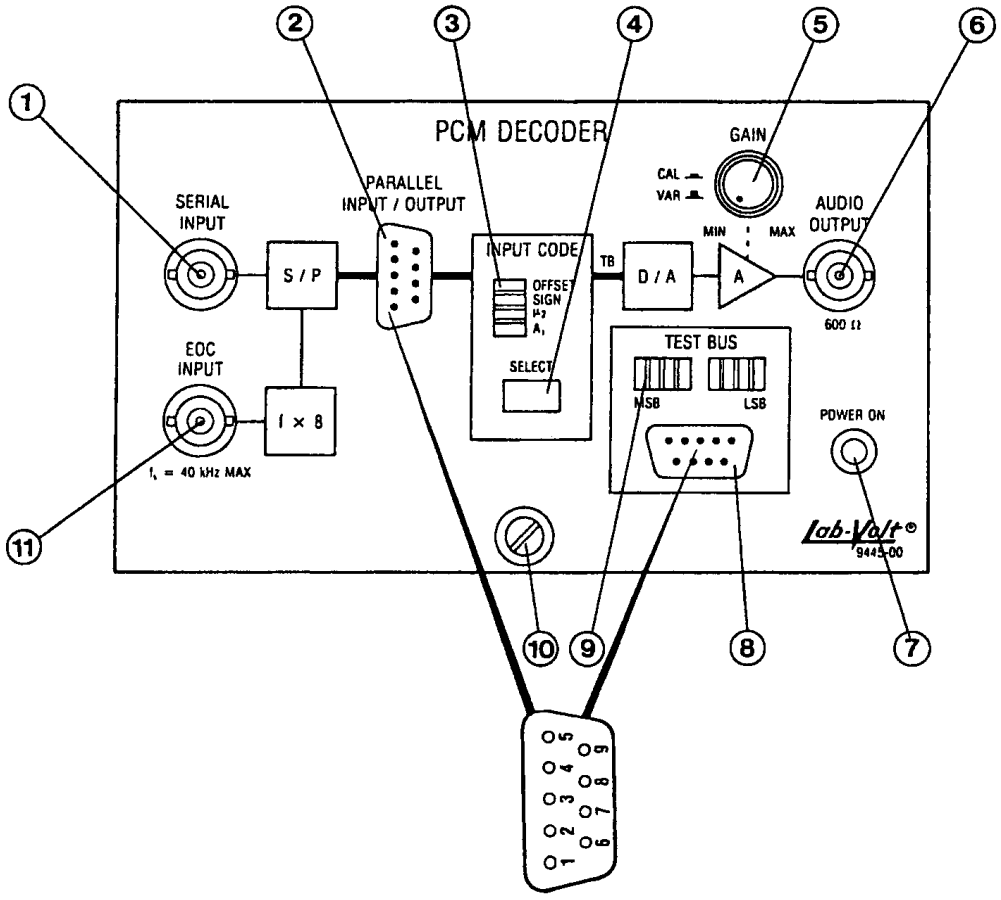

Figure 1. Front Panel of the PCM Decoder.

5 GAIN – Knob to set the overall gain of the PCM Decoder.

In the CALibrated position, the output signal voltage can vary between –2 V and +2 V for a PCM signal between 00 H and FF H.

Note: *The above data stands for an output with no load.*

In the VARiable position, the signal amplitude will range from 0 to 5 times the one obtained in the CALibrated position.

6 AUDIO OUTPUT – BNC connector to provide the output result of the D/A conversion.

7 POWER ON – This green LED lights when correct power is applied to the module.

8 TEST BUS OUTPUT – Nine-pin connection to provide the PCM signal at the input of the Digital-to-Analog converter.

9 TEST BUS MONITOR – Red LED display. This display shows the logic state of each of the eight bits of the test bus located at the input of the Enclosure / Supply Regulator.

10 THUMB-SCREW FASTENER – Secures the module to the Enclosure - Supply Regulator.

11 EOC INPUT – BNC connector to inject the signal to reconstruct the shift clock needed by the S/P converter. If the SERIAL INPUT is fed by the PCM Encoder, the EOC OUTPUT of the PCM Encoder must be connected to the EOC INPUT of the PCM Decoder.

SECTION 4

DESCRIPTION OF OPERATION

The PCM Decoder, Model 9445, consists mainly of a serial-to-parallel (S/P) converter, of a digital expander (ROM), and of a digital-to-analog (D/A) converter.

The PCM signal can be received in serial or parallel form. Sequential reception is through the SERIAL INPUT where the bit stream will be transformed in a parallel form PCM signal by a serial-to-parallel (S/P) converter. A frequency multiplier is used to restore a shift clock from the EOC signal. When the serial-to-parallel conversion is ended, buffer memory 1 stores the parallel form PCM signal. The output of the buffer memory 1 is sent to the input code ROM and to the PARALLEL INPUT / OUTPUT.

If the PCM signal is received in parallel form, it can be fed directly to the input code ROM via the PARALLEL INPUT / OUTPUT. When so, the output of buffer memory 1 must be disconnected. Disconnection is carried out by the EOC INPUT being without signal since the EOC signal controls the output of buffer memory 1.

The input code ROM contains four pre-programmed transfer functions: a linear function, a code converter, and two expanders. A selection circuit allows choice of functions and a LED display shows which one was selected.

The transition of each bit at the ROM output is synchronized by buffer memory 2 and the glitch eliminator. If no synchronization circuit is used, a noisy signal would otherwise result from the D/A conversion.

Digital-to-analog (D/A) conversion of the PCM signal is carried out by the D/A converter and its output amplifier.

All internal buses of this module are 8-bit buses.

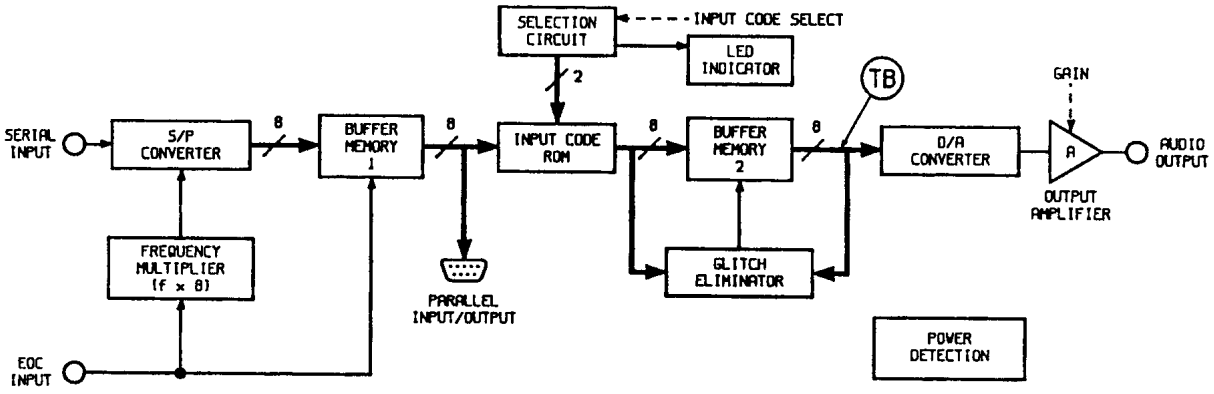

Figure 2. Block Diagram of the PCM Decoder.

SECTION 5

FAULT SWITCHES AND TEST BUS

5.1 Fault Switches

Fault switches enable the instruction to simulate faults for the teaching of troubleshooting. Access is through an opening in the transparent cover of the module. A fault is active when its switch is in the I position.

5.2 Fault Description

FAULTS CREATED BY THE FAULT SWITCHES

FLT 1 The S/P converter is disabled. Then, there is no output on the PARALLEL INPUT / OUTPUT.

FLT 2 The frequency multiplier multiplies only by 2. Then, only two clock cycles instead of eight are available to the shifting sequence.

FLT 3 The bit A5 of the input code ROM is disabled.

FLT 4 The MSB of the input code ROM is disabled.

FLT 5 The MSB of the input code ROM is replaced by the LSB. The switch swap the MSB with the LSB (A0) at the input code ROM causing the signal at the AUDIO OUTPUT to be distorted.

FLT 6 The selection circuit gives only two choices of input code. So, two of the four transfer functions of the ROM cannot be accessed.

FLT 7 The positive reference voltage of the D/A converter is changed.

FLT 8 The output amplifier is disabled. The switch grounds the AUDIO OUTPUT terminal preventing the output of any signal.

5.3 Test Bus (See Figure 2)

The test bus appearing on the front panel is identified below:

TB D/A Converter Input

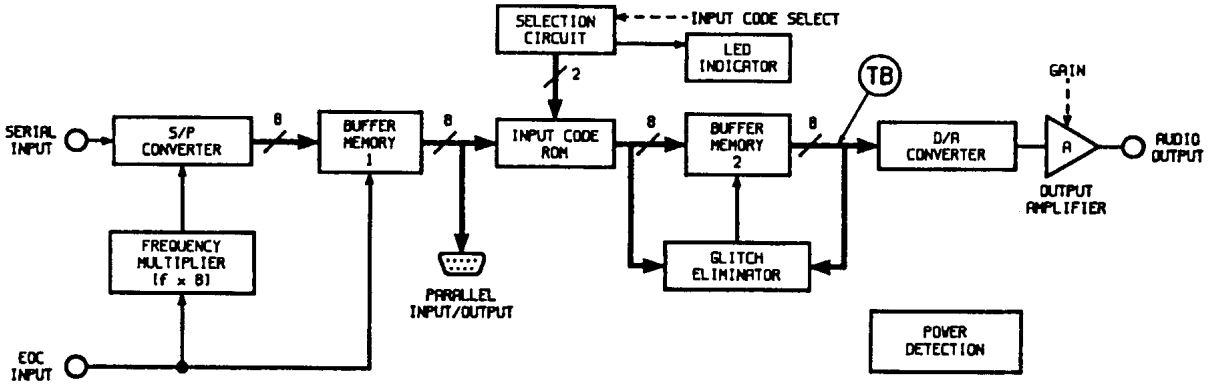

Figure 3. Location of the Test Bus.

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