

Programmable on-chip photonic signal processor based on a microdisk resonator array

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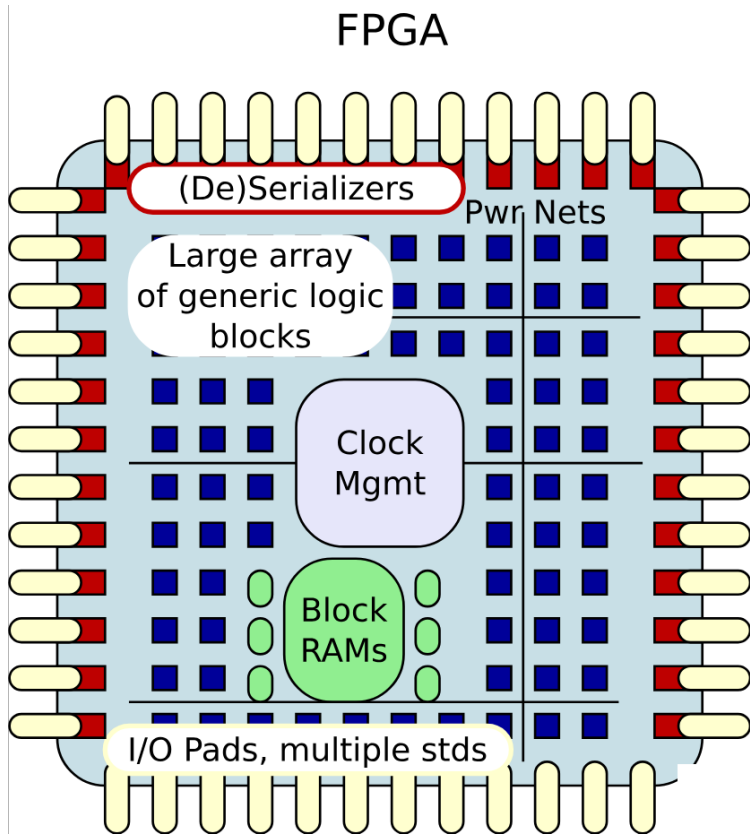
L'Université canadienne
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**MWP2018, Oct. 22-25, 2018
Toulouse, France**



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Introduction



A **field-programmable gate array (FPGA)** is an electronic integrated circuit designed to be configured by a customer after being manufactured.

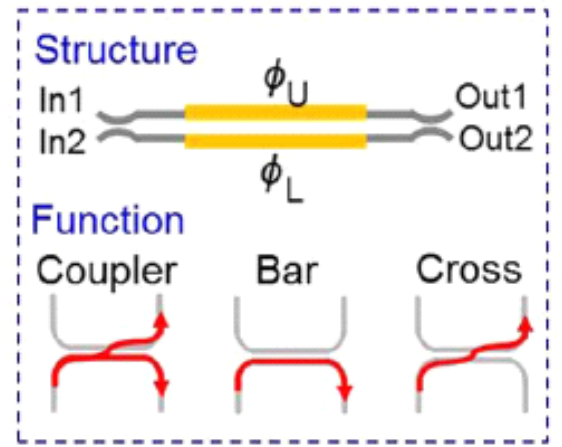
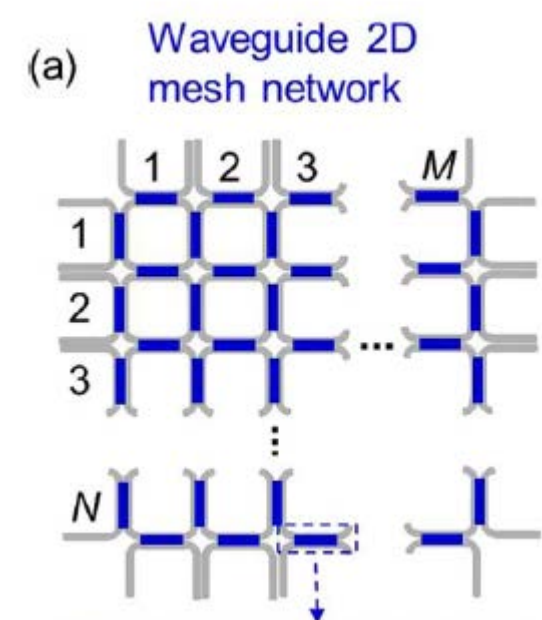
Can we have a photonic FPGA?



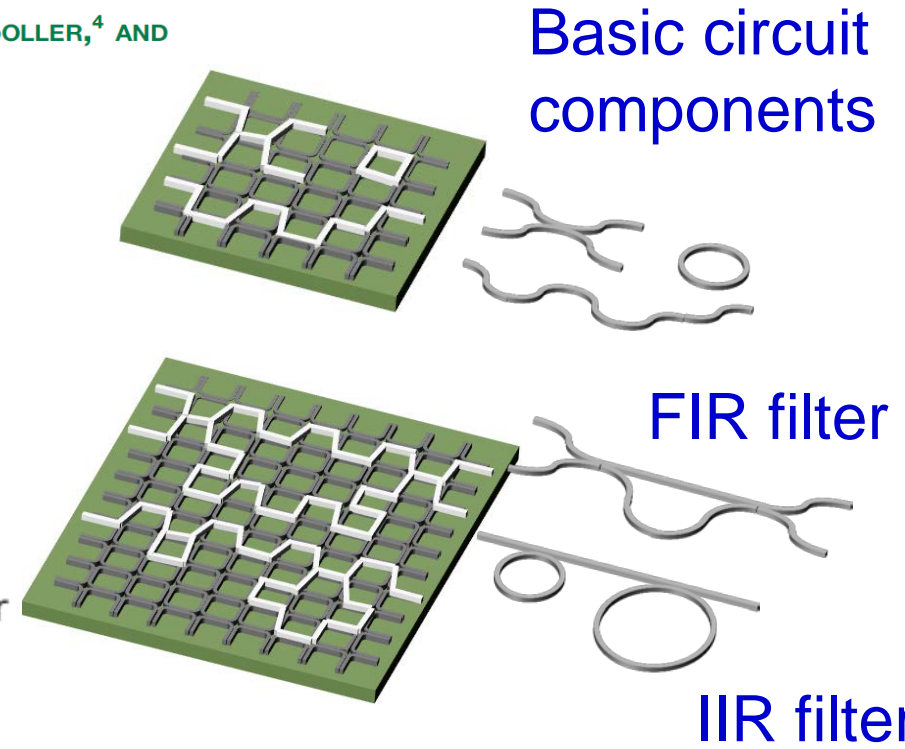
Programmable photonic signal processor chip for radiofrequency applications

LEIMENG ZHUANG,^{1,*} CHRIS G. H. ROELOFFZEN,² MARCEL HOEKMAN,³ KLAUS-J. BOLLER,⁴ AND ARTHUR J. LOWERY^{1,5}

Rectangular cell

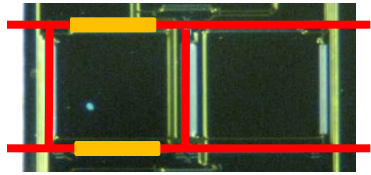


- Waveguide
- Mach-Zehnder coupler
- Phase tuning element
- Light propagation

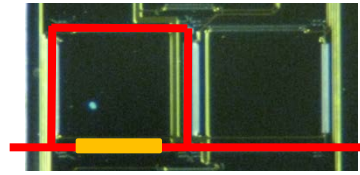
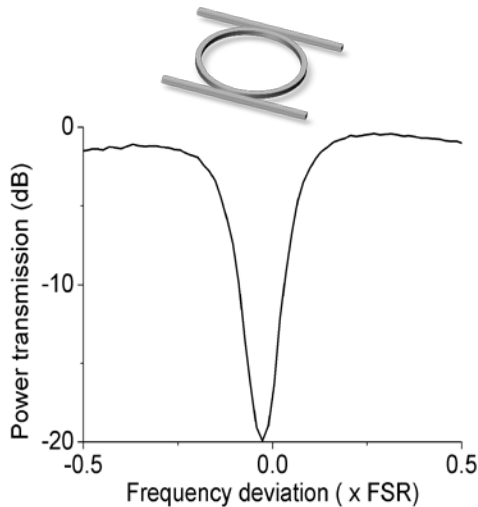


Proof-of-concept demonstration

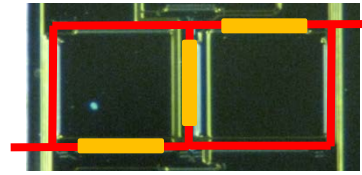
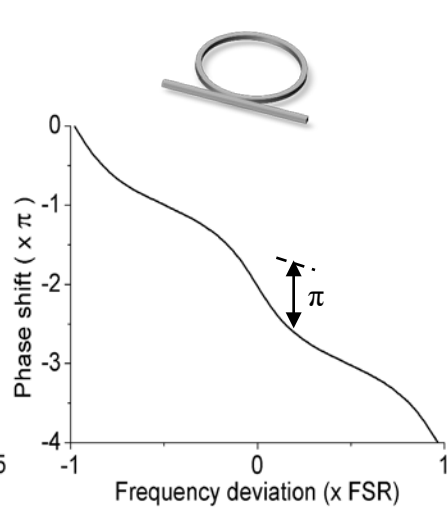
— Bar (switch)
— Coupler



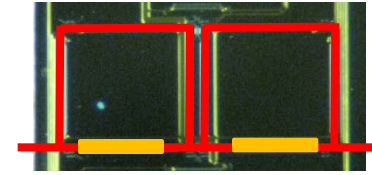
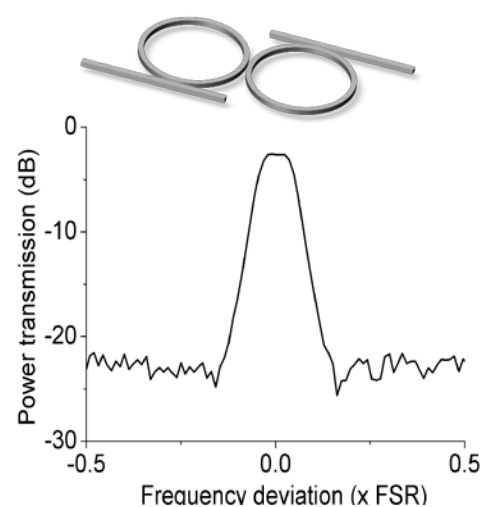
Notch filter



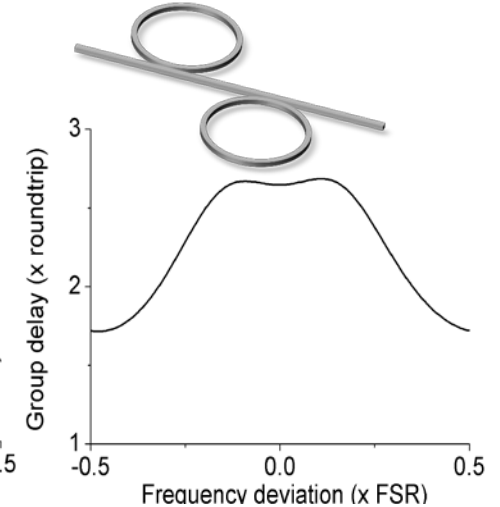
Hilbert transformer



Bandpass filter



Delay line



ARTICLE

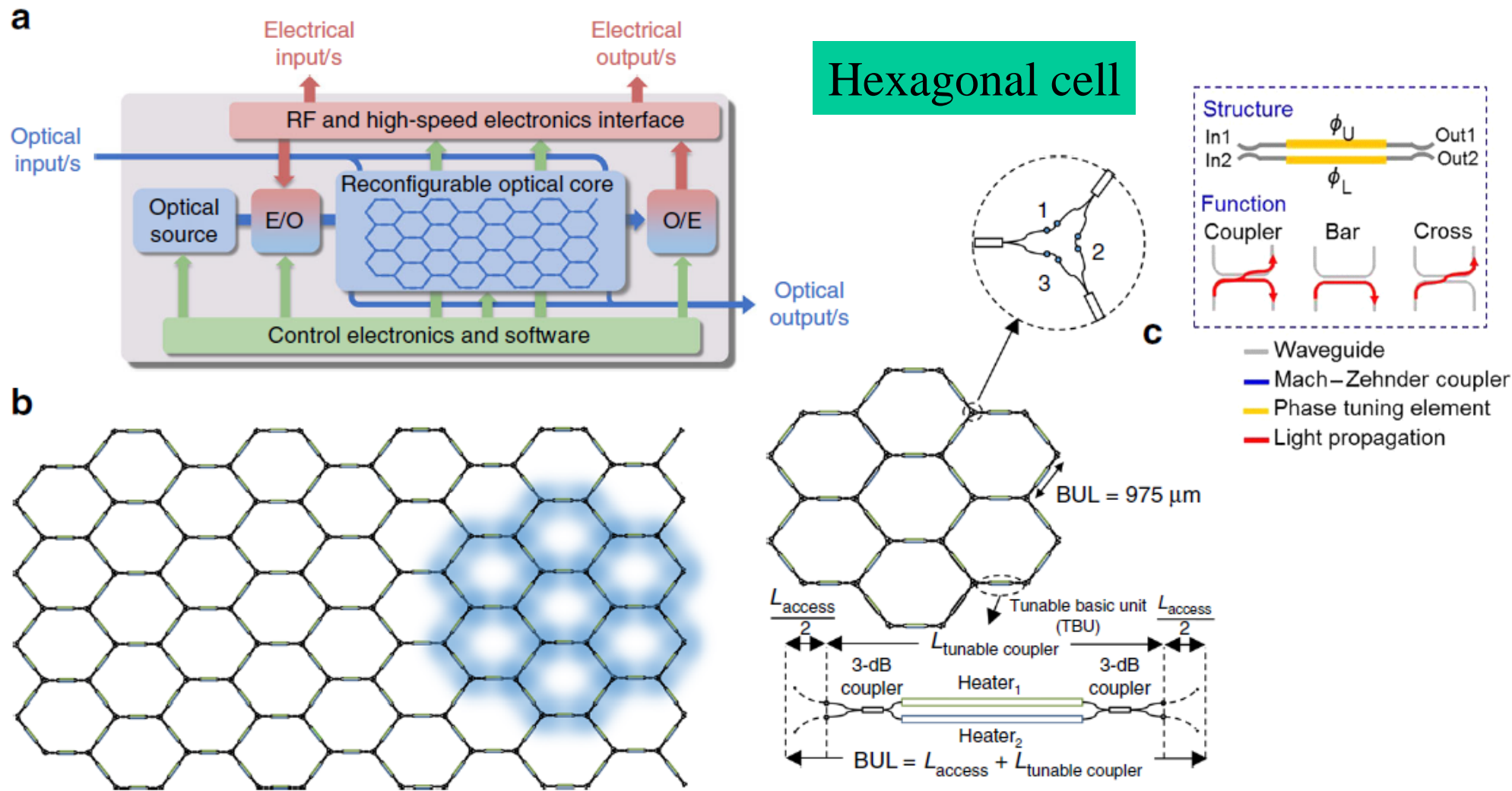
DOI: 10.1038/s41467-017-00714-1

OPEN

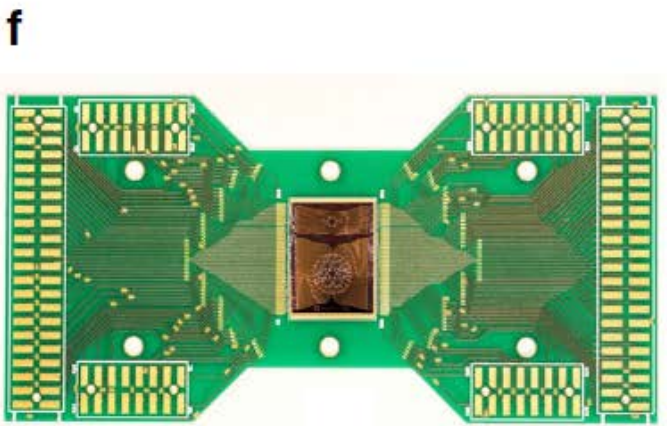
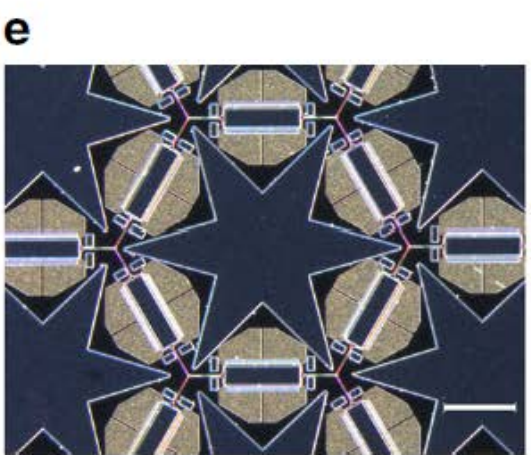
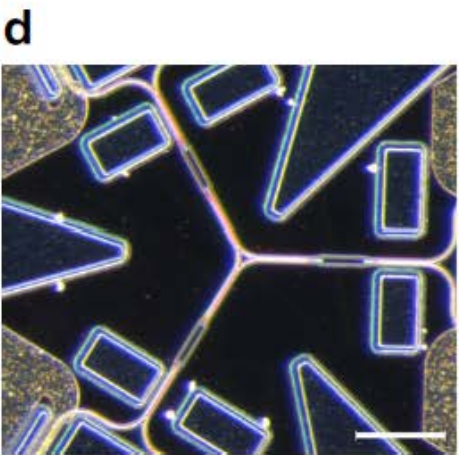
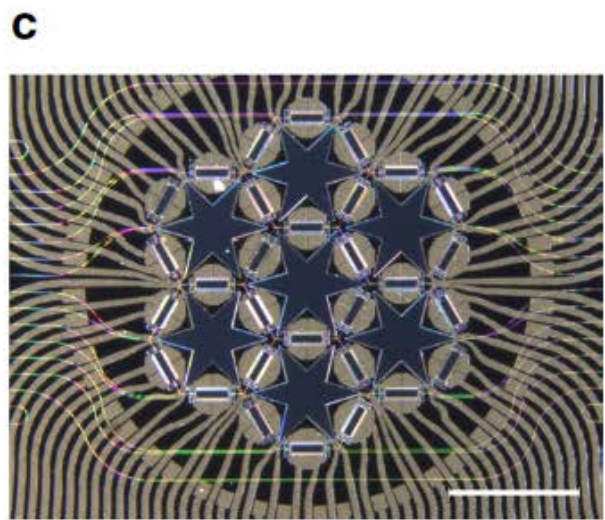
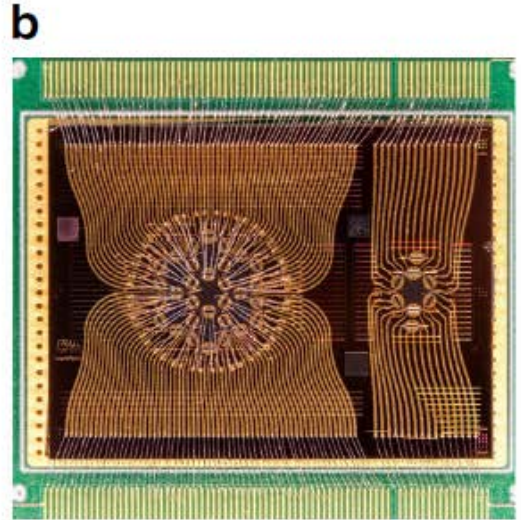
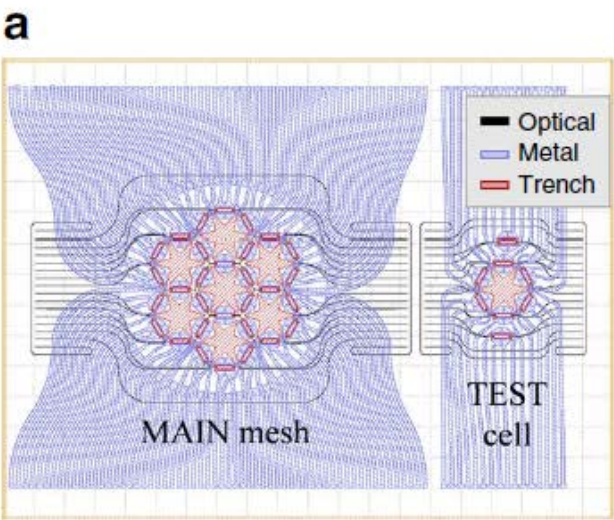
Multipurpose silicon photonics signal processor core

Daniel Pérez¹, Ivana Gasulla¹, Lee Crudginton², David J. Thomson², Ali Z. Khokhar², Ke Li², Wei Cao ², Goran Z. Mashanovich^{2,3} & José Capmany¹

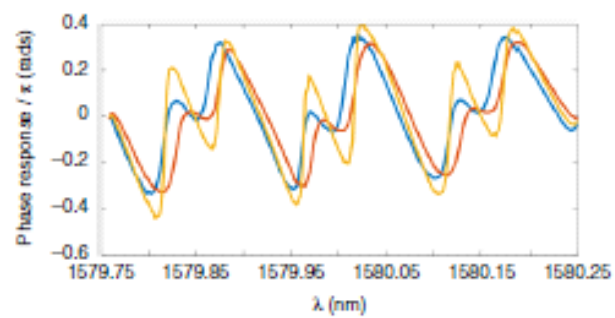
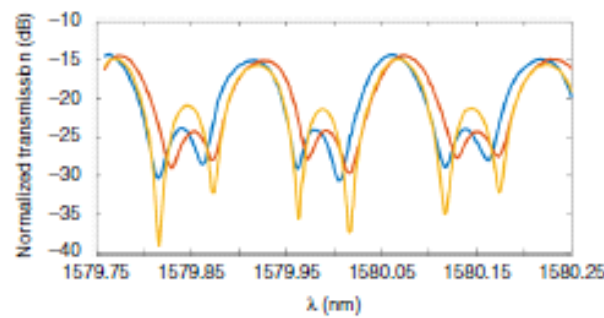
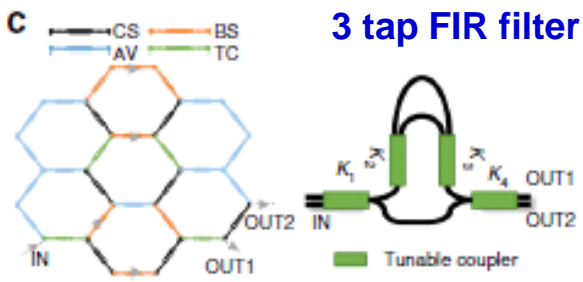
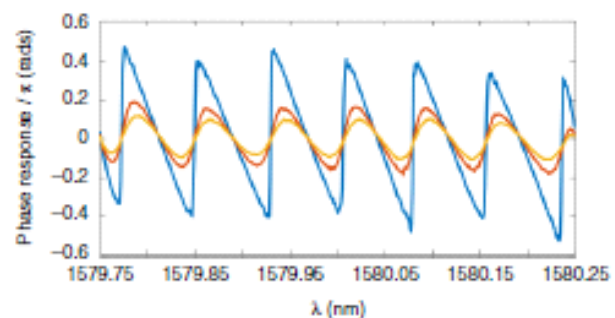
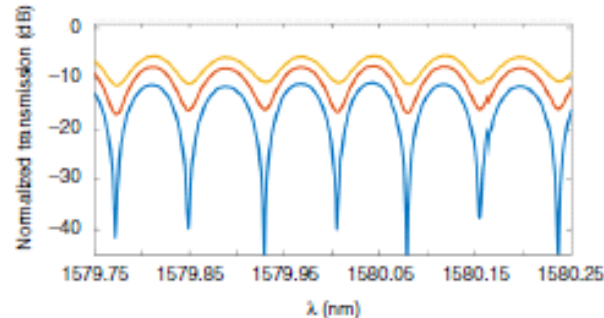
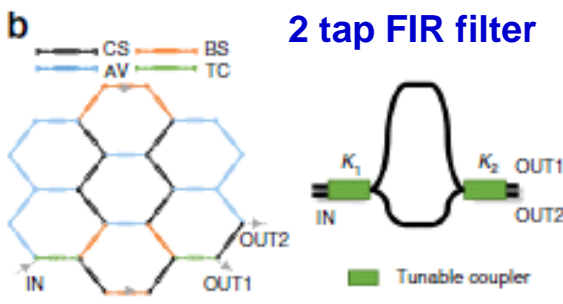
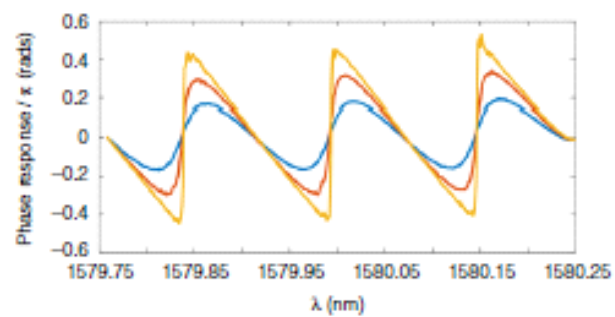
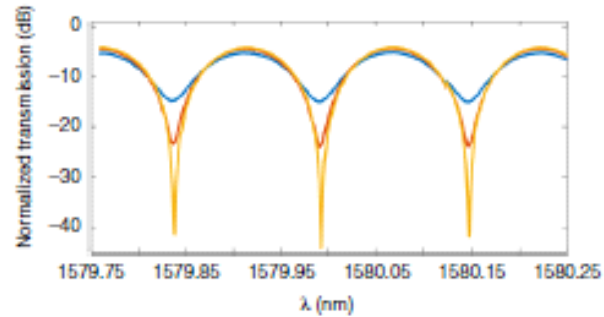
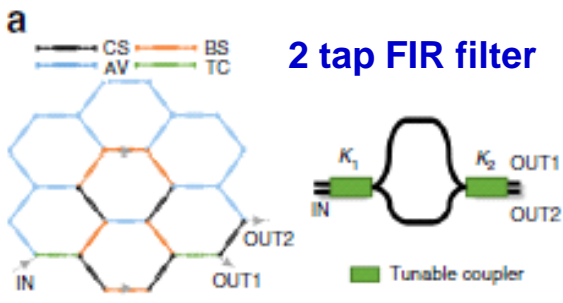
Introduction - Programmable photonic signal processors



Introduction - Programmable photonic signal processors



Introduction - Programmable photonic signal processors



Introduction

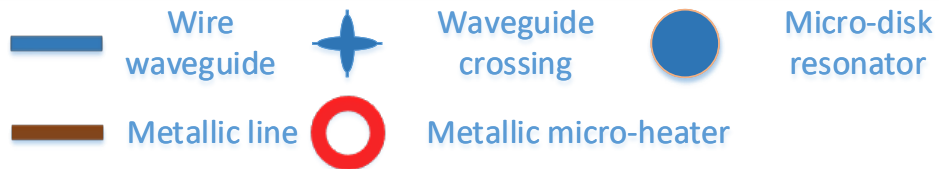
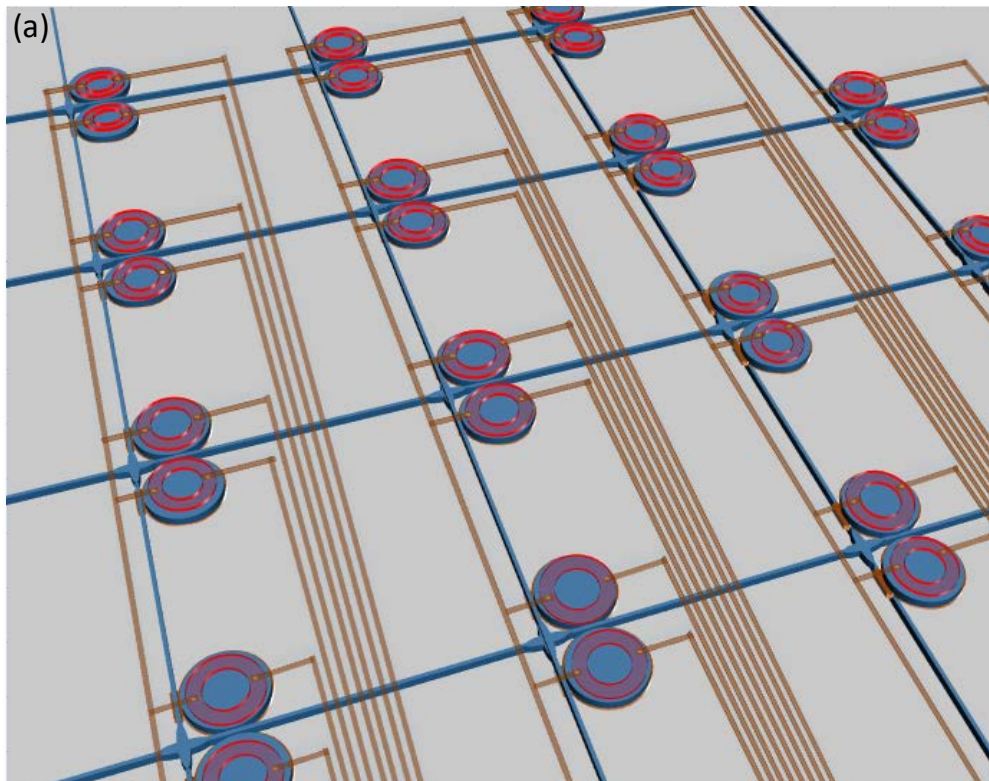
The architectures reported in the two previous papers

- has large size and high power consumption – small-scale integration
- less flexibility in reconfigurability

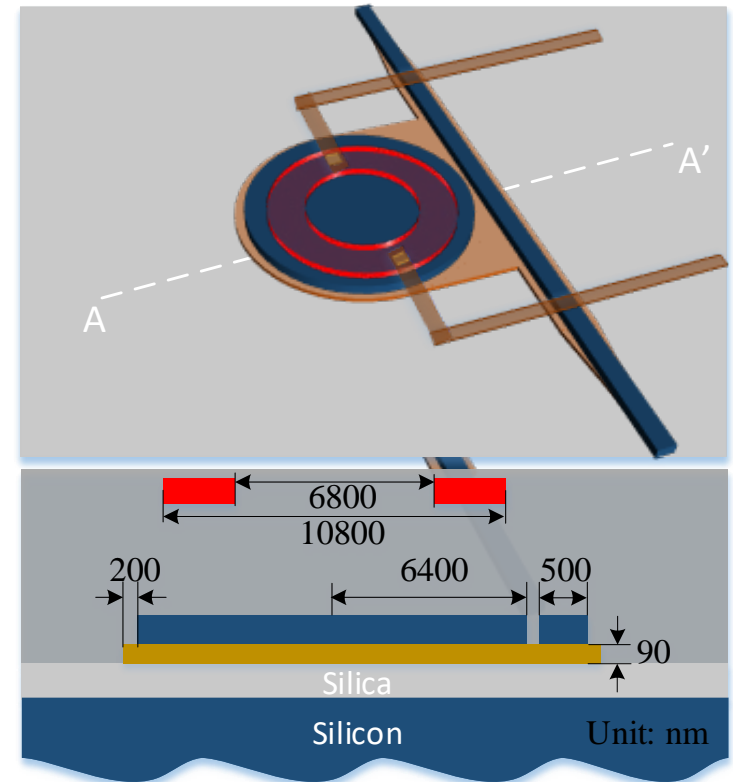
Solution: to change the rectangular or hexagonal cells to microdisk cells.



A disk-based large scale photonic FPGA



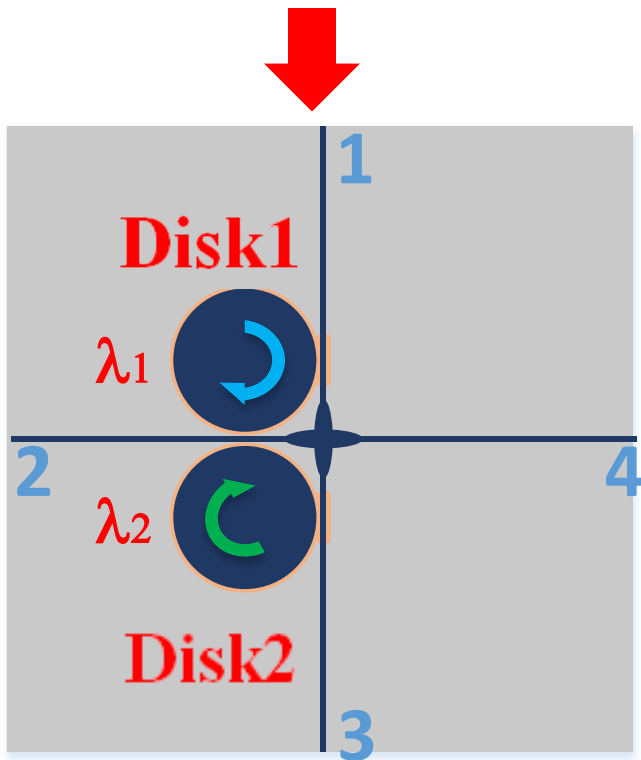
8 x 8 disk mesh network



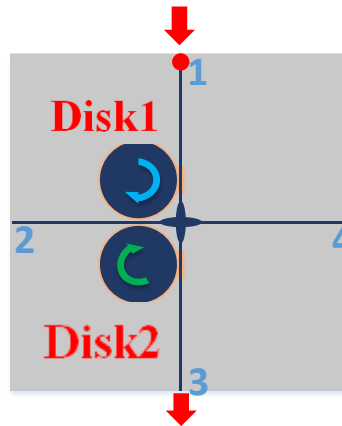
Much smaller size

Operation – signal routing

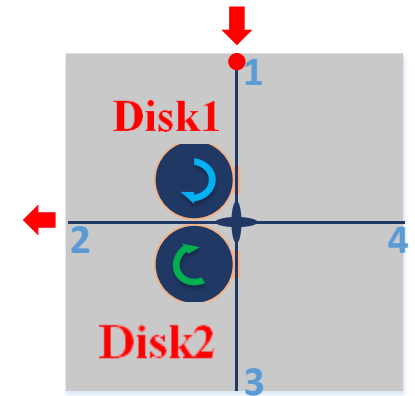
Input optical
signal λ_0



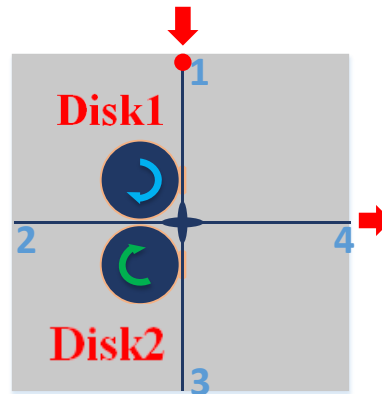
$\lambda_0 \neq \lambda_1 \neq \lambda_2$



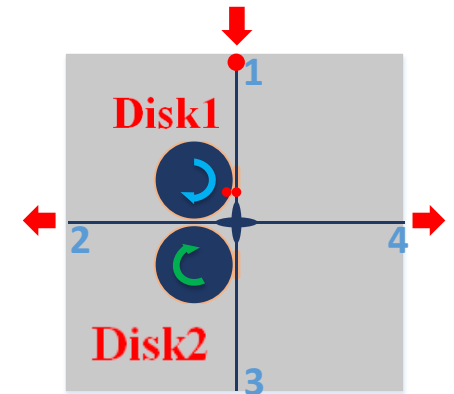
$\lambda_0 = \lambda_1 \neq \lambda_2$



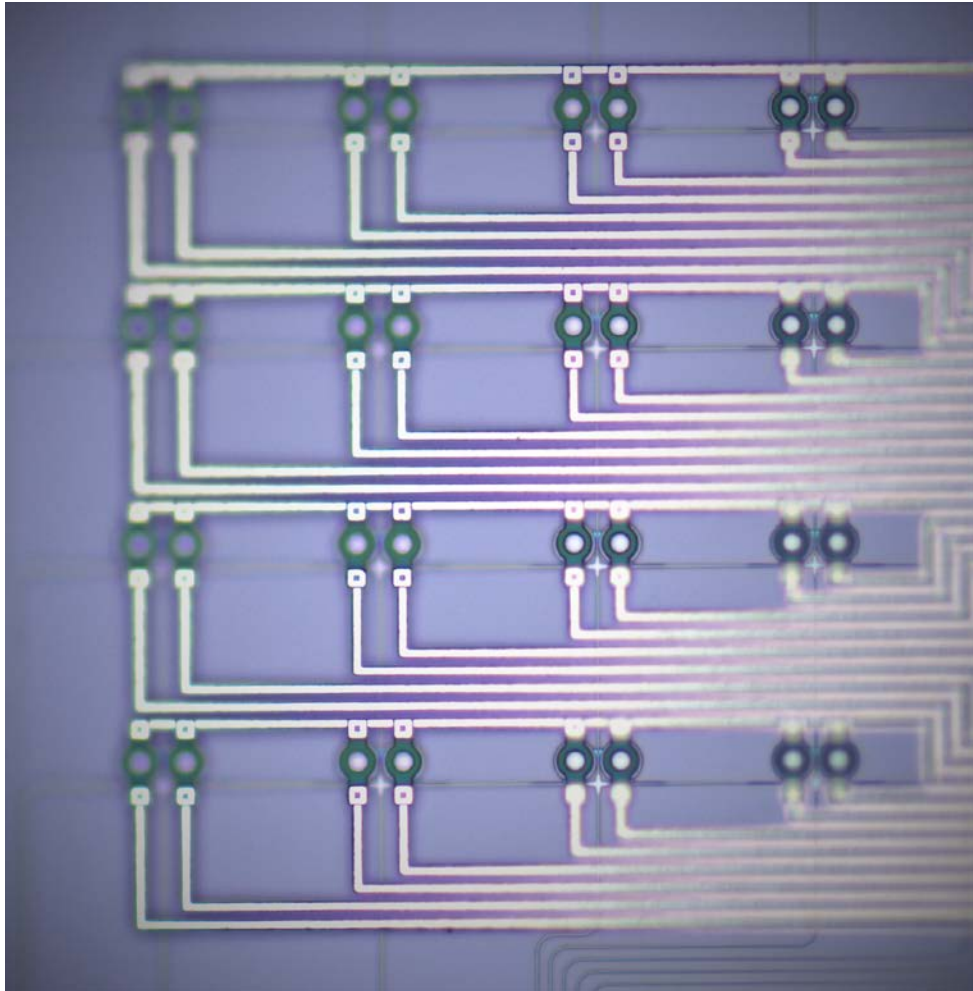
$\lambda_0 = \lambda_2 \neq \lambda_1$



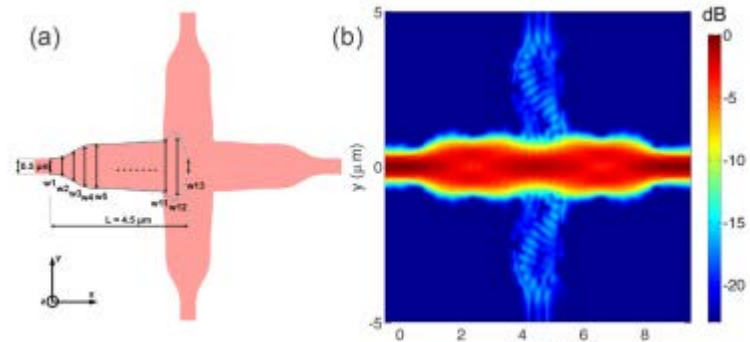
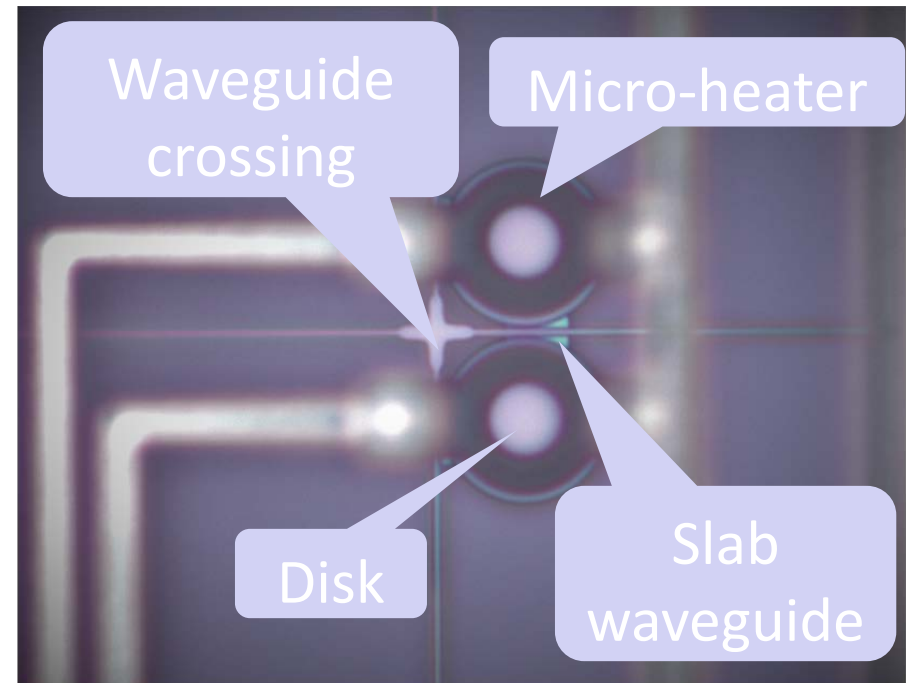
$\lambda_0 = \lambda_1 = \lambda_2$



Fabricated device

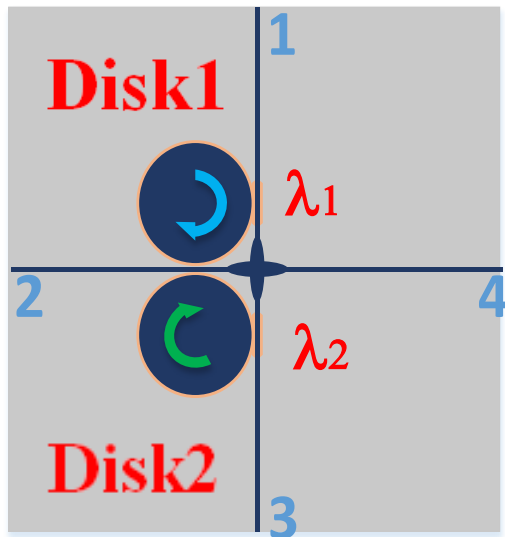
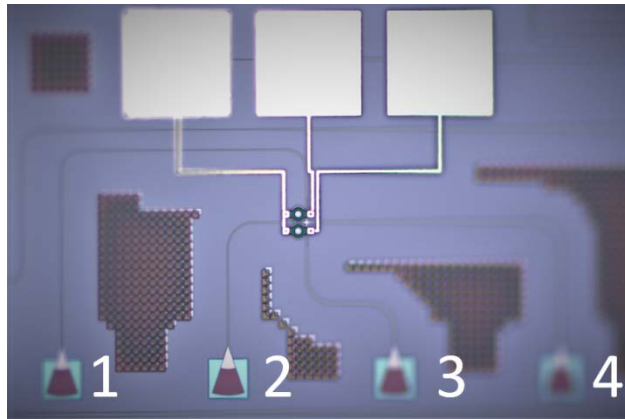


8 x 8 disk mesh network



Opt. Express 21, 29374-29382 (2013)

Measurements



2

3

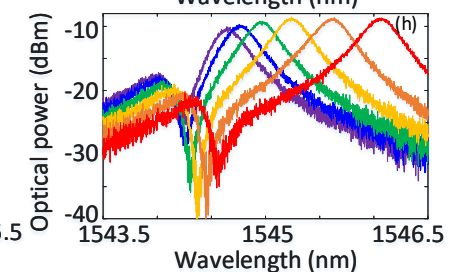
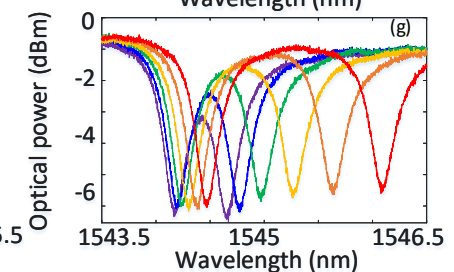
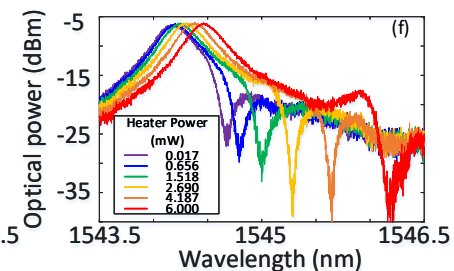
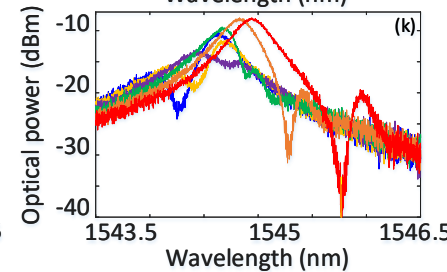
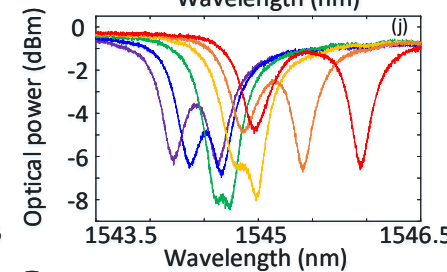
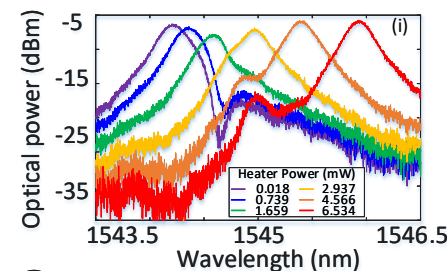
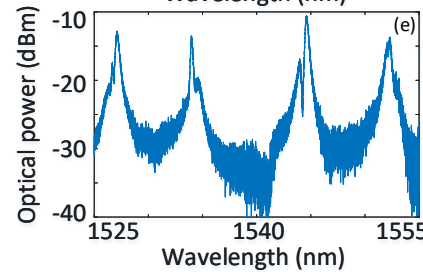
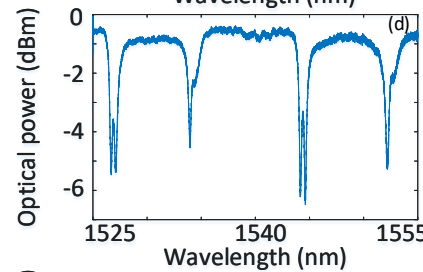
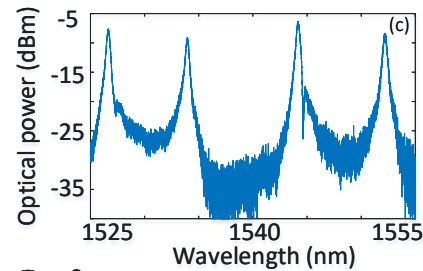
4

Port

Static State

Disk 1 is tuned

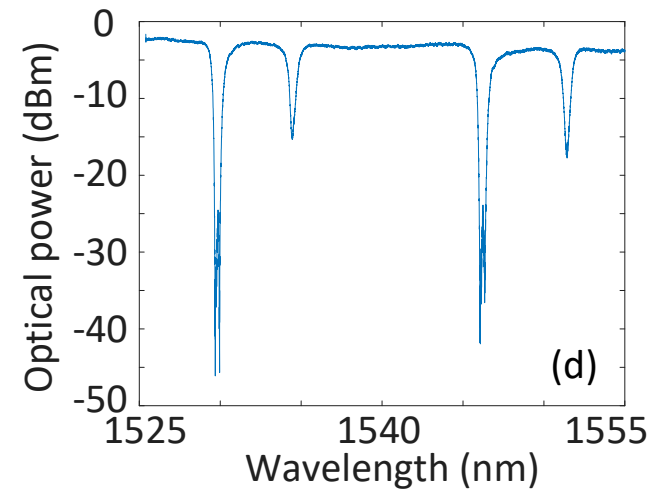
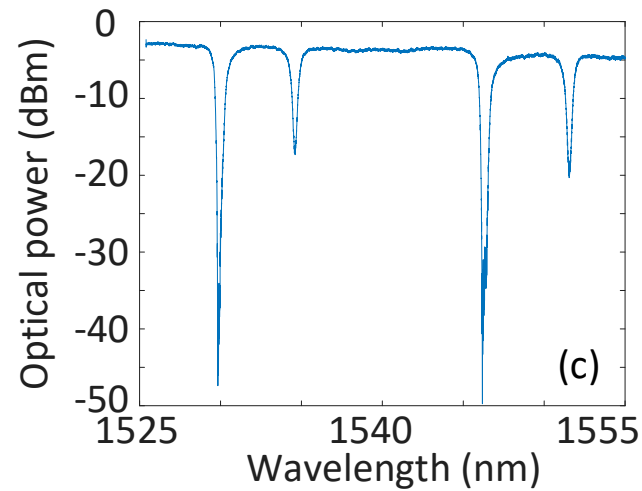
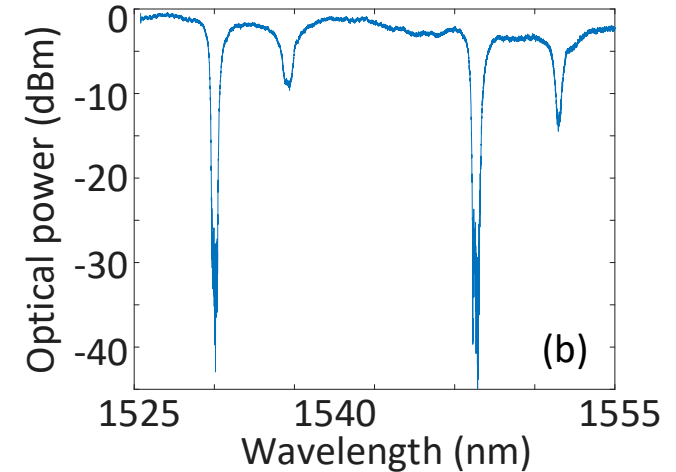
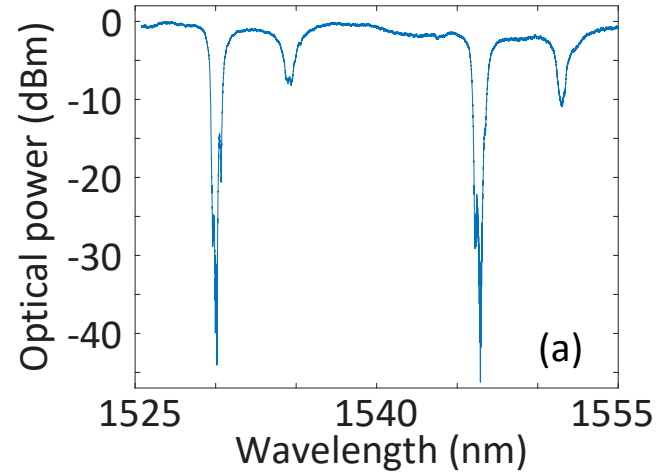
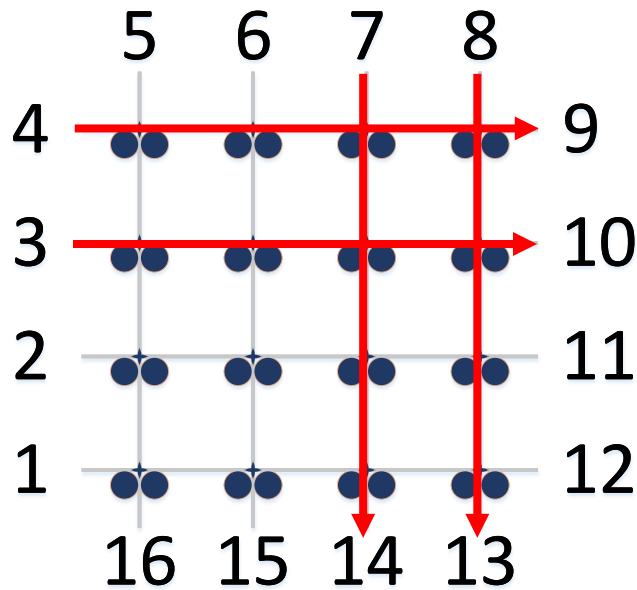
Disk 2 is tuned



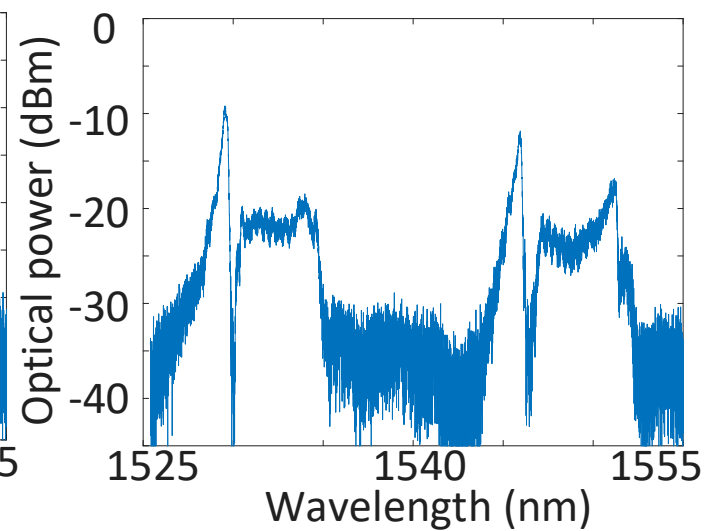
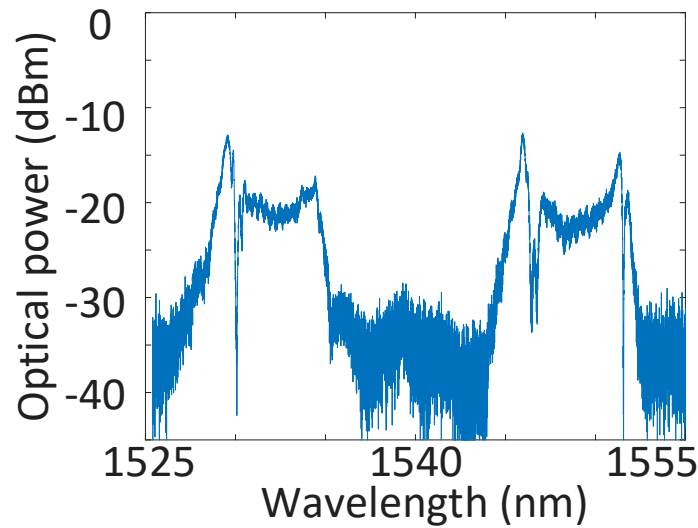
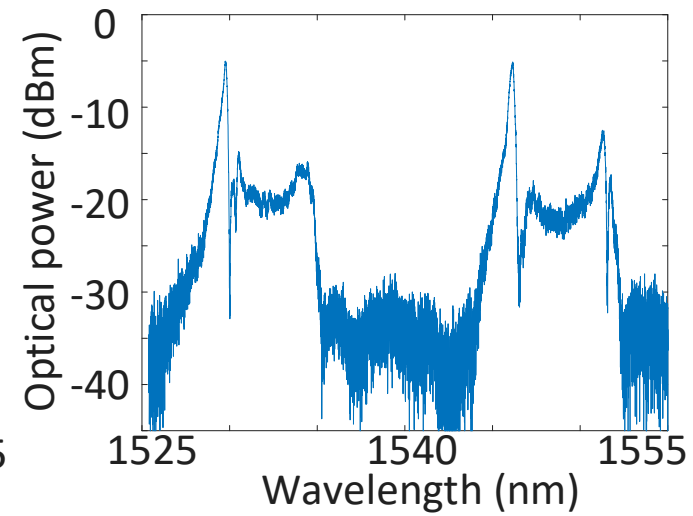
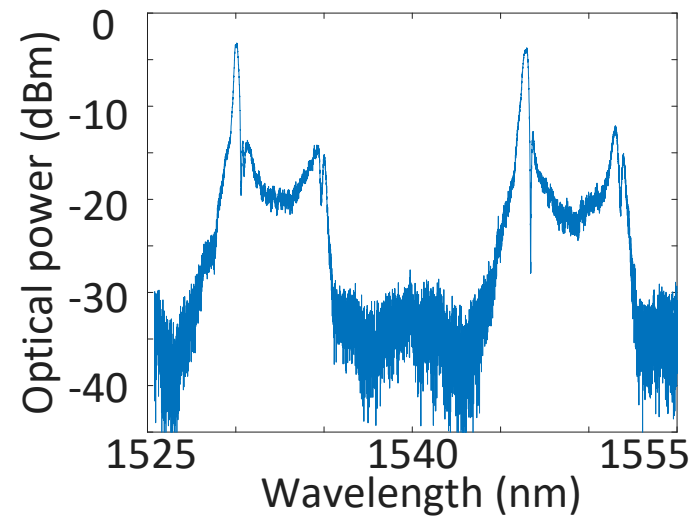
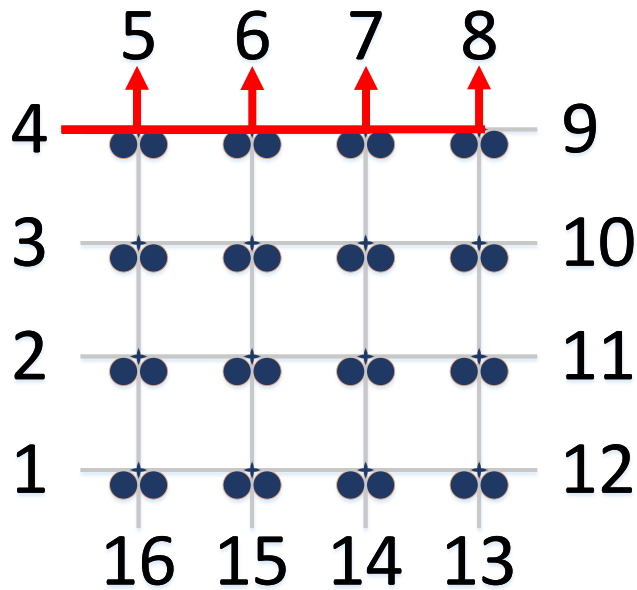
Measured by Luna OVA



Measurements

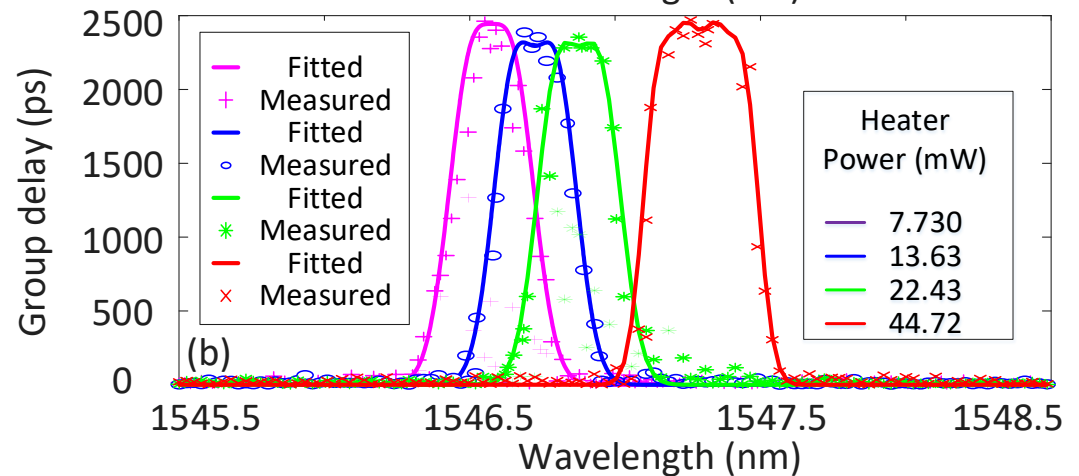
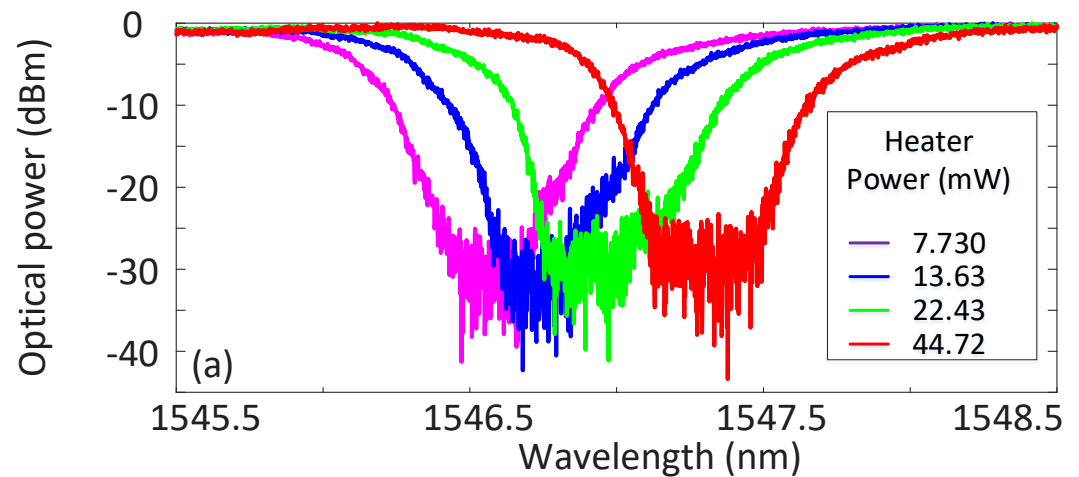
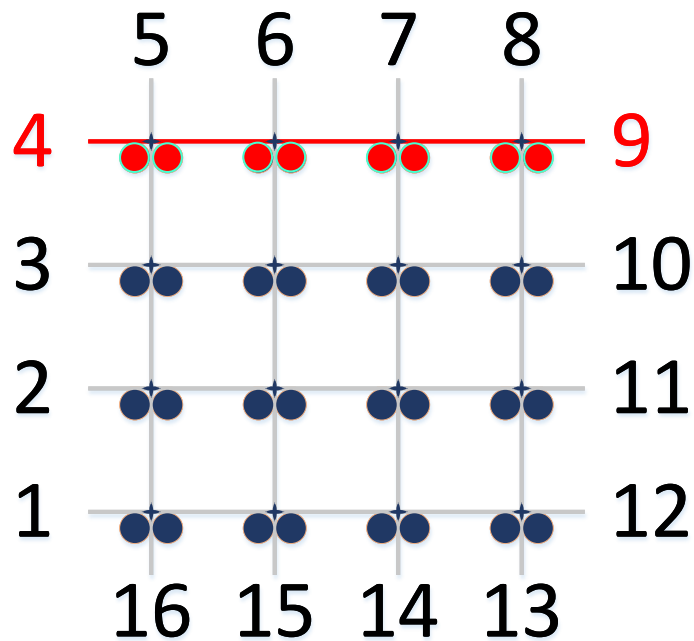


Measurements

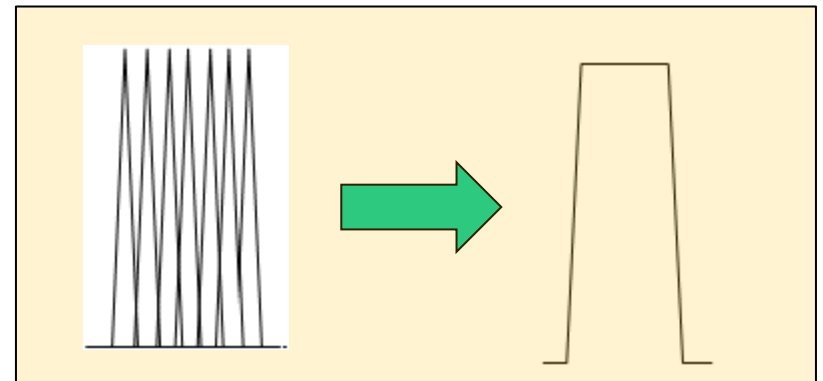
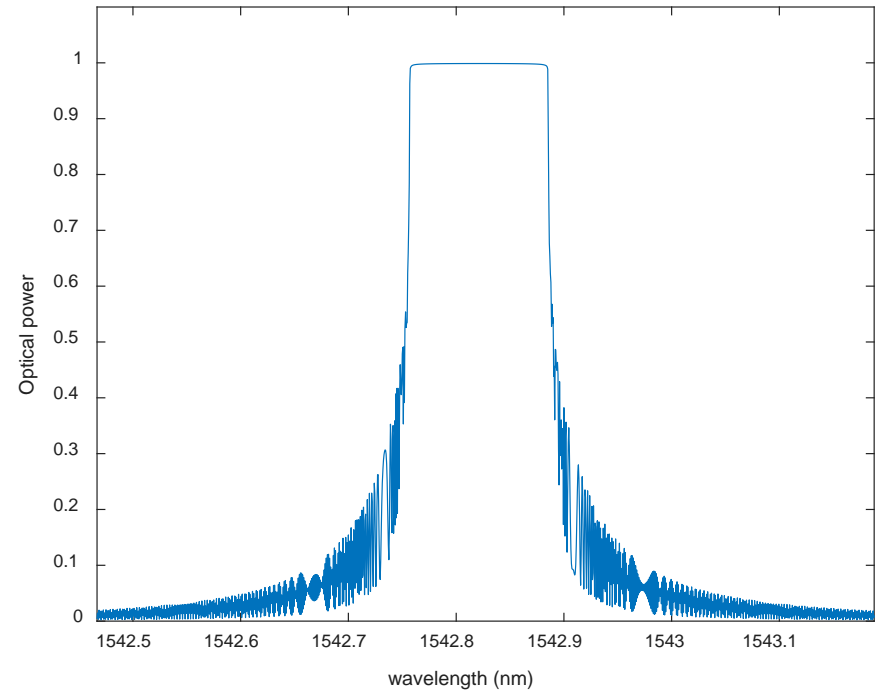
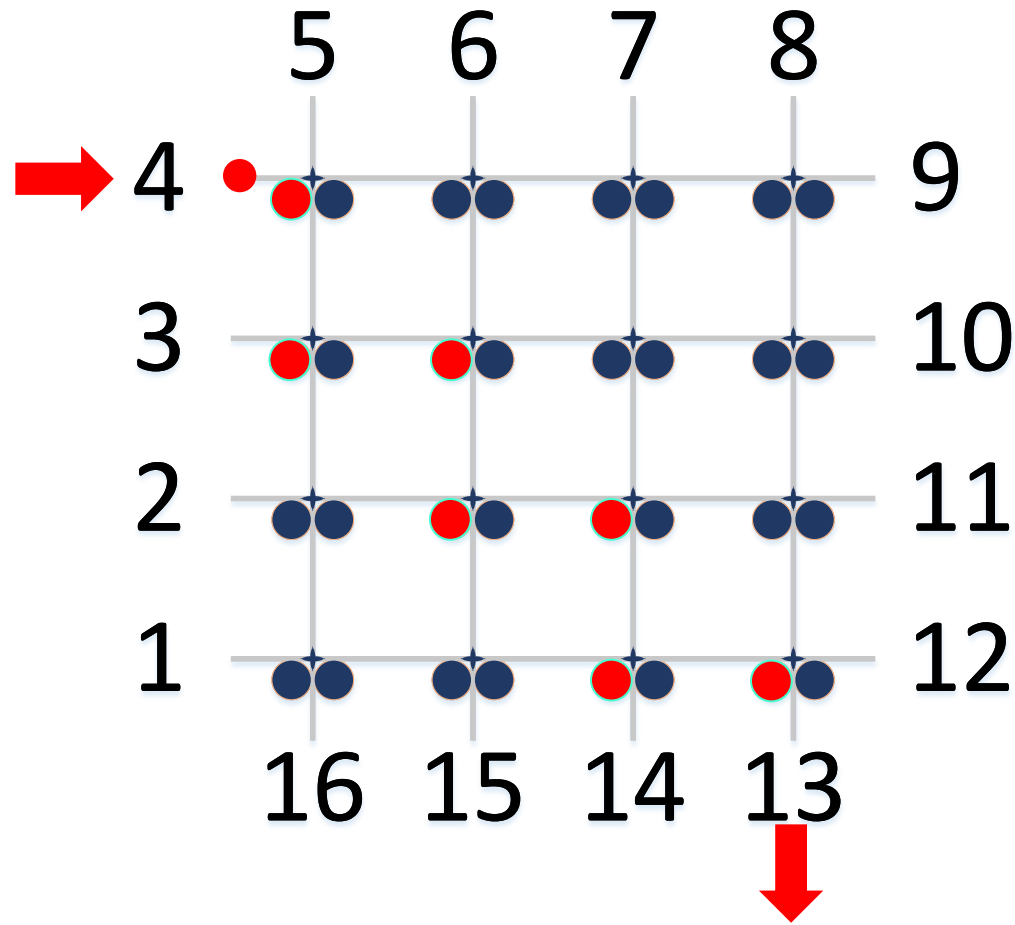


Delay-line demonstration

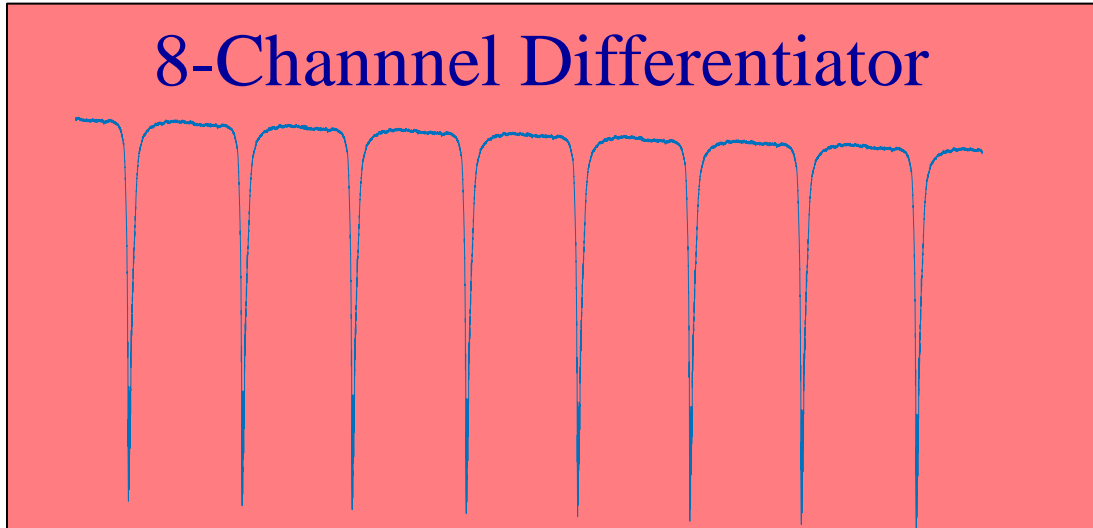
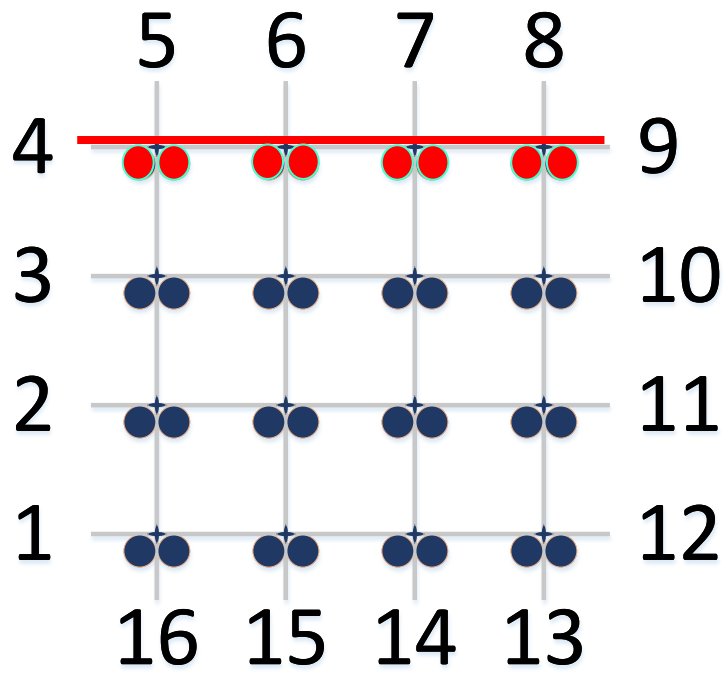
An on-chip tunable optical delay line based on 8 cascaded MDRs in all-pass filter configuration



Discussion: as a flat-top bandpass optical filter

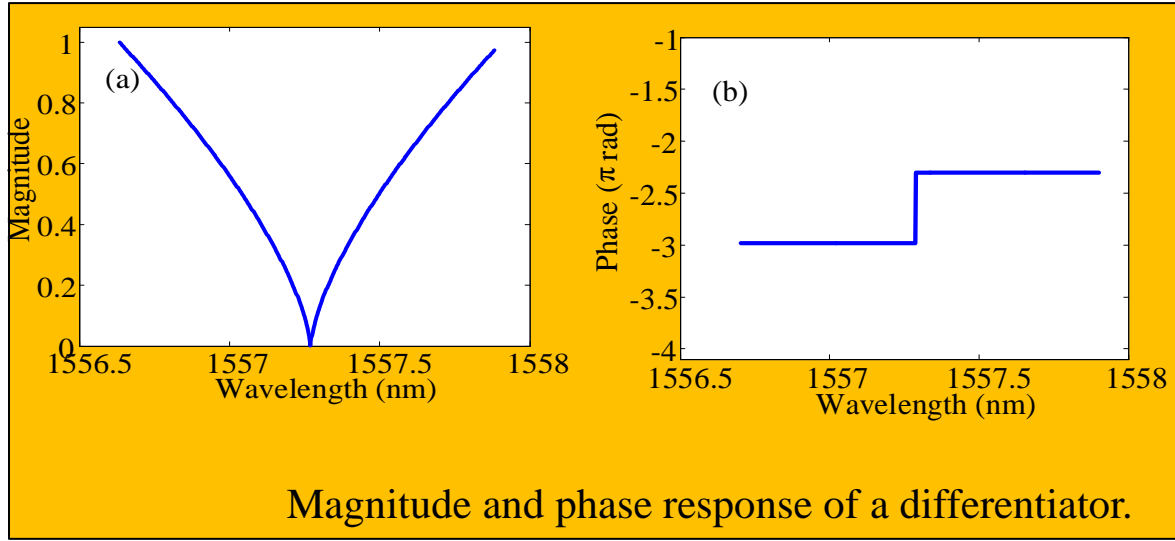


Discussion: as a multichannel differentiator - WDM systems

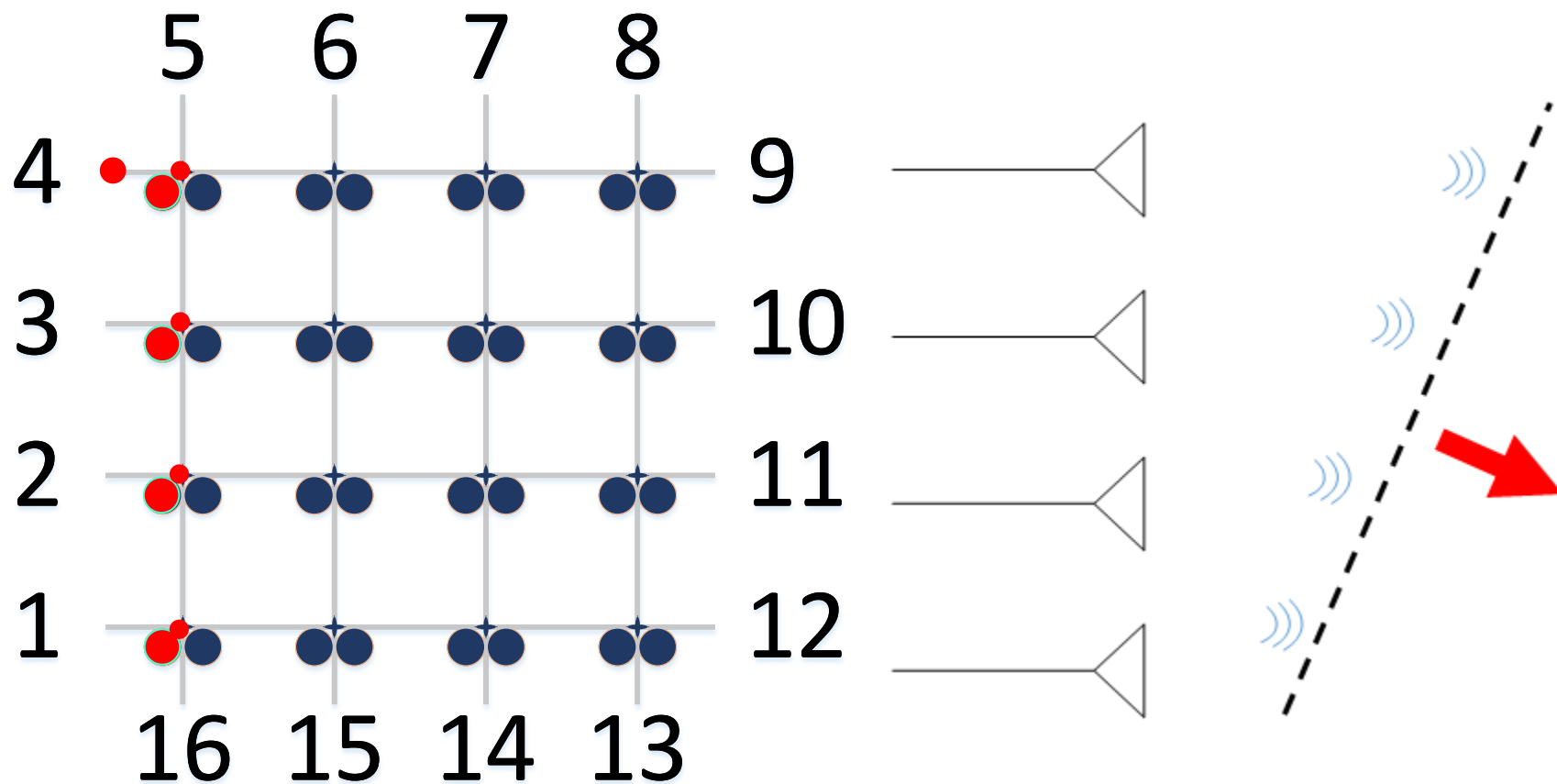


$$y(t) = \frac{dx(t)}{dt}$$

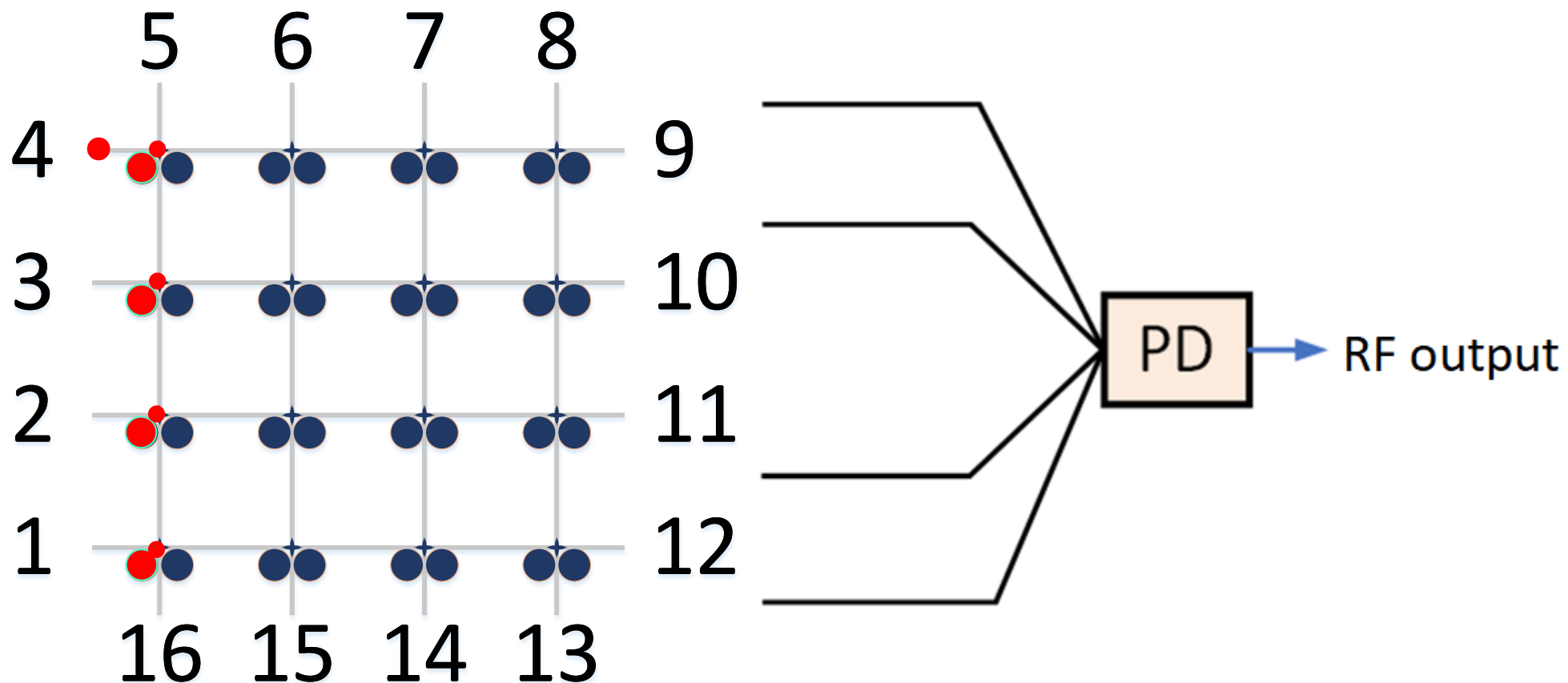
$$H(j\omega) = j(\omega - \omega_0) = \begin{cases} e^{j\frac{\pi}{2}} |\omega - \omega_0| & \omega > \omega_0 \\ e^{-j\frac{\pi}{2}} |\omega - \omega_0| & \omega < \omega_0 \end{cases}$$



Discussion: as an optical beamforming network



Discussion: as a delay line FIR filter



Conclusion

- ❑ A programmable photonic signal processor based on a silicon photonic microdisk array can be flexibly reconfigured and have a smaller size – suitable for large scale integration.
- ❑ The processor can be reconfigured to achieve diverse signal processing functions including time delay, temporal differentiation, true time delay beamforming, and microwave delay line filtering – an optical FPGA.

CMC Microsystems



NSERC Si-EPIC program



NSERC
CRSNG





Thank you and welcome to MWP2019 in Ottawa

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